CLAIMS

What is claimed is:

1. A method for sensing a signal received from an array cell within a memory array, the method comprising the steps of:

generating an analog voltage Vddr proportional to a current of a selected array cell of said memory array; and

comparing said analog voltage Vddr with a reference analog voltage Vcomp to generate an output digital signal.

2. The method according to claim 1, further comprising providing a reference unit with a reference cell having a similar structure and a similar current path therethrough to that of said array cell, and providing a drain driver for driving drain bit lines of said memory array and reference drain bit lines of said reference unit, wherein said drain driver generates the analog voltage Vddr.

3. The method according to claim 1, wherein if said analog voltage Vddr is greater than the reference analog voltage Vcomp then a low output digital signal is output, and if said analog voltage Vddr is not greater than the reference analog voltage Vcomp then a high output digital signal is output.

4. The method according to claim 1, further comprising:

discharging said memory array and said reference unit;

charging said memory array and said reference unit so as to generate an array cell signal and a reference signal, respectively, and a timing signal;

generating a read signal when said timing signal reaches a predefined voltage level; and

generating a sensing signal from the difference of said cell and reference signals once said read signal is generated.

5. A method for sensing a memory cell, the method comprising the steps of:

transforming a signal from a memory cell to a time delay; and

sensing said memory cell by comparing said time delay to a time delay of a reference cell.

6. The method according to claim 5, wherein said time delay comprises a digital signal delay.

7. The method according to claim 5, wherein comparing said time delay to the time delay of the reference cell comprises comparing at least one of rise and fall times of said time delays.

8. The method according to claim 5, wherein transforming the signal from the memory cell to the time delay comprises generating an analog voltage Vddr proportional to a current of said memory cell.

9. The method according to claim 8, wherein comparing said time delay to the time delay of the reference cell comprises comparing said analog voltage Vddr with a reference analog voltage Vcomp to generate an output digital signal.

10. Apparatus for sensing a signal received from an array cell within a memory array, the apparatus comprising:

a drain driver adapted to generate an analog voltage Vddr proportional to a current of a selected array cell of said memory array; and

a comparator adapted to compare said analog voltage Vddr with a reference analog voltage Vcomp to generate an output digital signal.

11. The apparatus according to claim 10, further comprising a reference unit with a reference cell having a similar structure and a similar current path therethrough to that of said array cell, wherein said drain driver is adapted to drive drain bit lines of said memory array and reference drain bit lines of said reference unit.

12. The apparatus according to claim 10, wherein said comparator compares said analog voltage Vddr with a reference analog voltage Vcomp and generates said output digital signal in the following manner:

if said analog voltage Vddr is greater than the reference analog voltage Vcomp then a low output digital signal is output, and if said analog voltage Vddr is not greater than the reference analog voltage Vcomp then a high output digital signal is output.

13. The apparatus according to claim 10, further comprising a data unit that receives said output digital signal.

14. Apparatus for sensing a memory cell comprising:

a driver adapted to transform a signal from a memory cell to a time delay; and

a comparator adapted to compare said time delay to a time delay of a reference cell.

15. The apparatus according to claim 14, wherein said time delay comprises a digital signal delay.

16. The apparatus according to claim 14, wherein said comparator compares at least one of rise and fall times of said time delays.

17. The apparatus according to claim 14, wherein said comparator compares said analog voltage Vddr with a reference analog voltage Vcomp and generates said output digital signal in the following manner:

if said analog voltage Vddr is greater than the reference analog voltage Vcomp then a low output digital signal is output, and if said analog voltage Vddr is not greater than the reference analog voltage Vcomp then a high output digital signal is output.